Self-Aligned Coupled Nanowire Transistor

Tero S. Kulmala,[†] Alan Colli,[‡] Andrea Fasoli,[†] Antonio Lombardo,[†] Samiul Haque,[‡] and Andrea C. Ferrari[†,*]

[†]Department of Engineering, University of Cambridge, Cambridge CB3 0FA, U.K. and [‡]Nokia Research Centre, Cambridge, U.K

ABSTRACT The integration of multiple functionalities into individual nanoelectronic components is increasingly explored as a means to step up computational power, or for advanced signal processing. Here, we report the fabrication of a coupled nanowire transistor, a device where two superimposed high-performance nanowire field-effect transistors capable of mutual interaction form a thyristor-like circuit. The structure embeds an internal level of signal processing, showing promise for applications in analogue computation. The device is naturally derived from a single NW *via* a self-aligned fabrication process.

KEYWORDS: nanowire · field-effect transistor · self-assembly · thyristor

The continuous downscaling of feature sizes in Si microelectronics faces fundamental and technological barriers.[1−3] Bottom-up nanostructures, such as carbon nanotubes or semiconductor nanowires (NWs), could play an important role in overcoming the limit where high-resolution lithography is no longer viable.[3,4] These nanostructures can operate as field-effect transistors (FETs), with good performance.[4−6] The challenge arises when moving from prototype devices toward integrated systems. Here the assembly and registration of close-packed nanocomponents becomes increasingly difficult.[7−12] Boolean logic devices were achieved using architectures consisting of NW-FETs.[13] Now the target is to realize devices allowing for some level of internal computation.[14,15] Reconfigurable junctions,[14,15] built-in NW heterostructures,[16,17] or memristors[18] are all promising examples of integration of more and novel functionalities into elementary nanocomponents.

Nanowire lithography (NWL) has emerged as a powerful combination of bottom-up and top-down methods.[19−24] It uses chemically grown NWs as masks to transfer their one-dimensional morphology into layers of well-defined properties and composition. NWL has been successfully applied to metals,[19,20] Si,[21] and graphene.[22,23] The most attractive feature of this approach is the formation of a self-aligned structure with two NWs superimposed for their whole length, a geometry very difficult to achieve by nanomanipulation or nanoassembly. However, in NWL the masks are normally sacrificial:[20,21] they either are removed at the end of the fabrication process[20] or play no active role in the final device.[21] Instead, this double-NW structure could be best exploited if the NW masks would be active, *i.e.*, introducing an additional function rather than being merely morphological templates. As an example, in the FET devices reported in refs 25 and 26 NWs act as etch masks to yield conformal graphene nanoribbon FET channels, as well as thin high-κ gate dielectrics. Electrically active NWs have also been used to gate graphene FETs while acting at the same time as evaporation masks to yield channel lengths down to ~130 nm.[24] In all these cases, however, the authors aimed to ease the fabrication and enhance the performance of a single conventional FET, while no additional circuitry or functionality was integrated into the structure.

Here, we use NWL to fabricate a coupled nanowire transistor (CNWT), an architecture integrating two mutually interacting FETs into a thyristor-like circuit. Thyristors are nonlinear electronic devices comprising, in their basic form, a stack of 3 pn junctions.[27] Our CNWT corresponds to a complementary metal-oxide semiconductor (CMOS) thyristor, an important electronic component for the realization of low-power delay elements in integrated circuits.[28] Electrical functionalities beyond those of a simple switch are therefore embedded in a single nanoscale component that is naturally formed *via* a self-aligned process, rather than assembled from the macroscopic world.

RESULTS AND DISCUSSION

Figure 1a,b show a schematic of the CNWT fabrication process (see Methods for details). We use Si as a test system. We previously utilized fully oxidized SiNWs for NWL on Si,[21] because SiO_2 provides excellent selectivity for Si deep reactive-ion etching (DRIE).[21,29] However, a Si/SiO_2 core/shell NW (with SiO_2 shell thicknesses as small as

* Address correspondence to acf26@cam.ac.uk.

Received for review March 30, 2011 and accepted August 3, 2011.

Published online August 03, 2011
10.1021/nn201203s

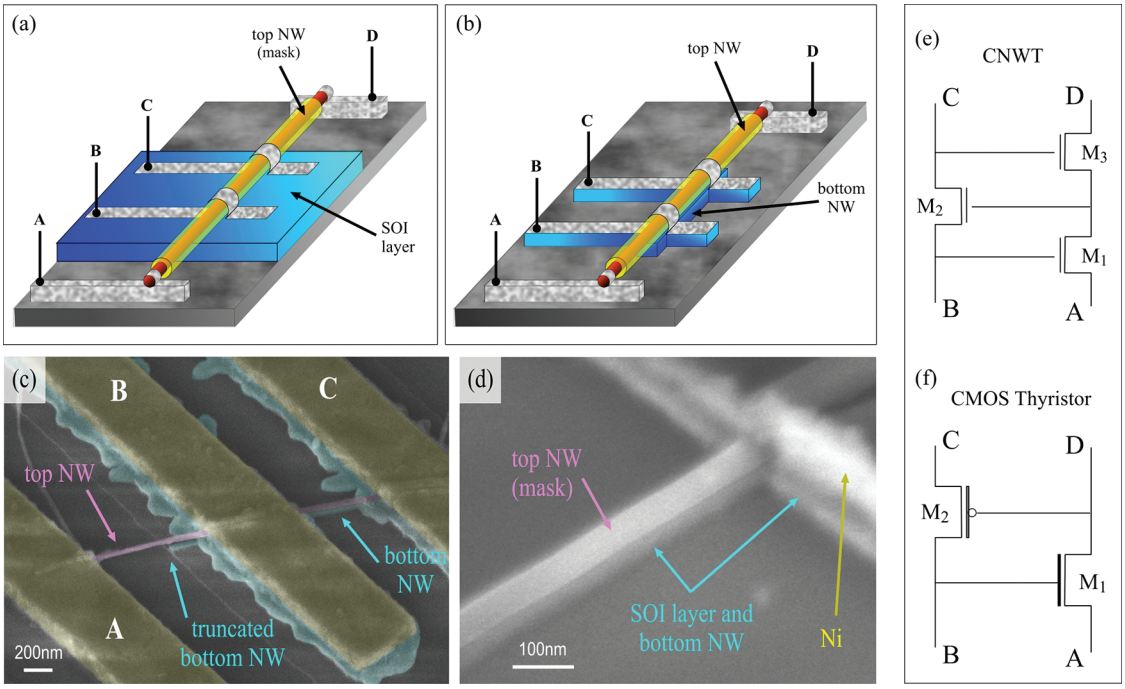

Figure 1. CNWT fabrication process. (a) An intermediate step, before anisotropic etching, is used to etch the silicon-on-insulator (SOI) device layer. The top-NW core is contacted at the NW ends. (b) The top-NW acts as etch mask, its morphology being reproduced in the underlying Si layer. Note that the D electrode is added for electrical characterization purposes only, but is not an essential component of our device. (c) False-color SEM micrograph of a representative device. (d) High-magnification SEM image of the stacked NWs within the device. (e) Schematic CNWT electric circuit: two FETs are integrated in the self-aligned, stacked NW architecture. (f) Circuit diagram of a CMOS thyristor.

10 nm) can as well be used as a suitable mask for Si etching, up to several hundreds of nanometers in depth, while the Si core remains protected and unaffected by the process (see Methods). Hence, we grow a Si/SiO_2 core/shell NW by vapor transport[30] and then transfer it onto an ultrathin (50 nm) silicon-on-insulator (SOI) wafer[21] (Figure 1a). Metal contacts (B and C) are deposited on the SOI layer and on the core/shell NW mask, so that after DRIE (Figure 1b) a SiNW channel (bottom-NW) is formed below the NW mask (top-NW). Because of the insulating shell surrounding the top-NW, there is no direct electrical contact between the two stacked NWs. Two outer electrodes are also deposited to contact the core of the top-NW (A and D). For this purpose, both the underlying SOI layer and the SiO_2 protective shell are locally removed prior to deposition of the A and D terminals. By using double-dose e-beam lithography,[31] it is possible to pattern all contacts in a single step (see Methods for details). Figure 1c shows a scanning electron microscope (SEM) image of a representative device, and Figure 1d a high-magnification image of the NW arrangement within the device. We note that our approach is not limited to Si/SiO_2 heterostructures. Indeed, various other NWs consisting of a semiconducting core and an insulating shell (*e.g.*, Ge/Al_2O_3[5] or ZnO/MgO[32]) could in principle be used as top-NWs, provided that the shell is not attacked by the etching process.

Figure 1e illustrates the CNWT equivalent circuit. The top-NW is used as interconnect to gate the bottom-NW FET (B, C) *via* a voltage applied to terminal A (or D, given the symmetry of the structure). However, since terminals B and C are capacitively coupled to the top-NW *via* the SiO_2 insulating shell, they can act as gates for the top-NW, effectively controlling its electrical properties. As a result, the gating of the bottom-NW induced by the voltage applied at A (or D) would strongly depend on how the bias is applied between terminals B and C (Figure 1e). The circuit diagram of a CMOS thyristor is illustrated in Figure 1f[28] and shows similarities to the CNWT structure. Note that in Figure 1e we do not define the polarity of the individual FETs since, in principle, the doping of the SOI film and of the top-NW can be independently controlled, allowing for a number of different combinations. The CMOS thyristor is thus only one example of a possible CNWT equivalent circuit.

We now examine the independent electrical response of the top and bottom NWs. We consider a case of undoped NW masks and a lightly boron doped SOI (resistivity 20 Ωcm). Figure 2 shows that charge transport in both NWs can be modulated using a common back-gate (*i.e.*, the Si substrate of the SOI). When measuring the conductance through the top-NW (A–D), terminals B and C are left floating (Figure 2a). Similarly, while measuring the conductance through the bottom-NW (B, C), terminals A and D are left floating

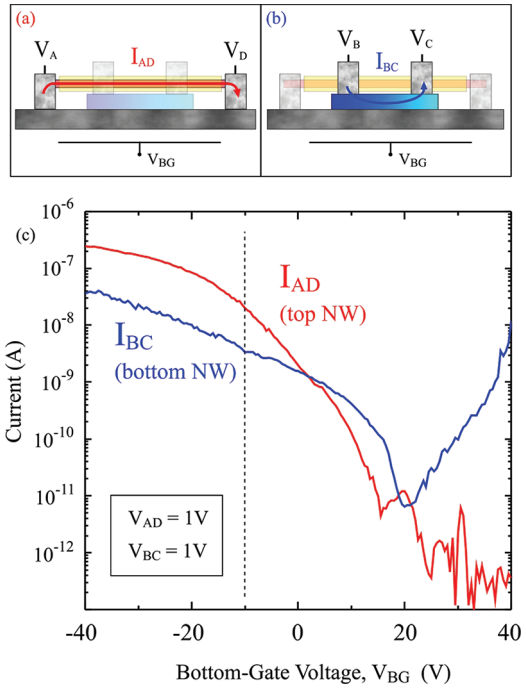

Figure 2. (a, b) Schematics of electrodes used for I_{AD} and I_{BC} measurements. Floating electrodes are plotted semitransparent. (c) Transfer curves as a function of V_{BG} when top- and bottom-NWs are operated independently. The top-NW (red curve) has p-type behavior. The bottom-NW (blue curve) is ambipolar.

(Figure 2b). The top-NW exhibits p-type behavior (red curve), since its valence band is pinned to the Fermi level of the metal contacts.[30,33,34] The bottom-NW shows ambipolar behavior (blue curve), consistent with what was previously observed for similar NWL-defined structures.[21] Using the common back-gate, on/off ratios of at least 10^4–10^5 are measured. To have simultaneous conduction in both NWs, we operate them in the hole-accumulation regime by applying a sufficiently negative back-gate voltage (−10 to −20 V), but still away from the saturation region (−30 to −40 V). This voltage range makes the NWs most responsive to external fields, thus mutual coupling is strongest.

We now show how charge transport in the top-NW (A–D) can be affected by V_B. In this configuration electrode B acts as a top-gate for the top-NW channel. Terminal C is left floating, so that, at equilibrium, $V_C = V_B$. Figure 3a plots the top-NW current, I_{AD}, as a function of V_B for different back-gate voltages. Here, V_A = 1 V and terminal D is grounded. Consistent with a p-type behavior, I_{AD} decreases for positive top-gate voltages. With the thin (∼10 nm) oxide shell playing the role of a gate dielectric, a relatively small voltage (2 V) is sufficient to fully switch off the FET.[31] An on/off ratio greater than 10^6 and a subthreshold slope of ∼150 mV/dec are obtained, comparable with those of state-of-the-art NW FETs.[5,31,33,35] Note that the back-gate strongly affects the saturation ON current (varying from 10^{-10} to 10^{-7}A), but has little influence on the

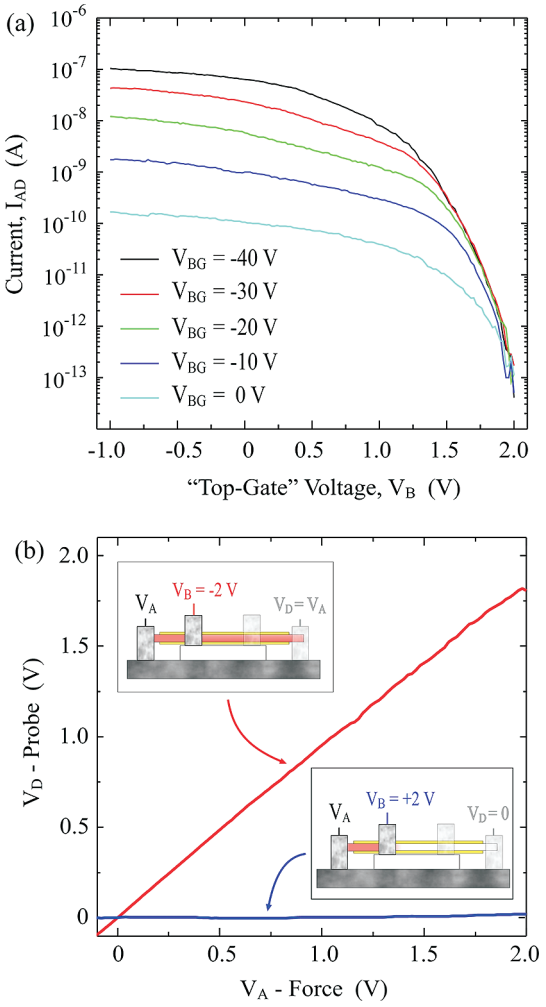

Figure 3. Effect of V_B on the top-NW conductance. (a) Top-NW I_{AD} as a function of V_B, for different V_{BG}. As V_B increases, I_{AD} decreases. For each curve, a $V_B \approx 2$ V can efficiently suppress the top-NW conductance. (b) Voltage propagation in the top-NW for $V_B = \pm 2$ V. The voltage is applied to A and sensed at D. For $V_B = +2$ V no V_D modulation is observed as V_A is swept.

threshold voltage. The top-NW was characterized both before (Figure 1a) and after (Figure 1b) DRIE. No degradation in conductivity was observed.

In Figure 3b terminal D is no longer grounded, and a voltage probe is used to read its potential (V_D), while V_A is swept from 0 to 2 V. If V_B is kept at −2 V, the top-NW channel is on (Figure 3a). The current is therefore allowed to flow in the top-NW, and V_D follows the voltage applied at electrode A. If V_B is kept at 2 V, the top-NW channel is OFF (Figure 3a). Charge transport is thus hindered in the top-NW beyond electrode B, and no potential can be built at terminal D ($V_D = 0$ for every V_A). This demonstrates that, for V_B = 2 V or higher, the voltage applied to terminal A cannot be transferred to the top-NW section between B and C, *i.e.*, where gating of the bottom-NW channel takes place. Indeed, Figure 4a shows that the efficiency of top-gating the bottom-NW (B, C) *via* the NW mask through terminal A strongly depends on V_B. If the top-NW is on (V_B = −2 V), V_A modulates the bottom-NW conductance, consistent

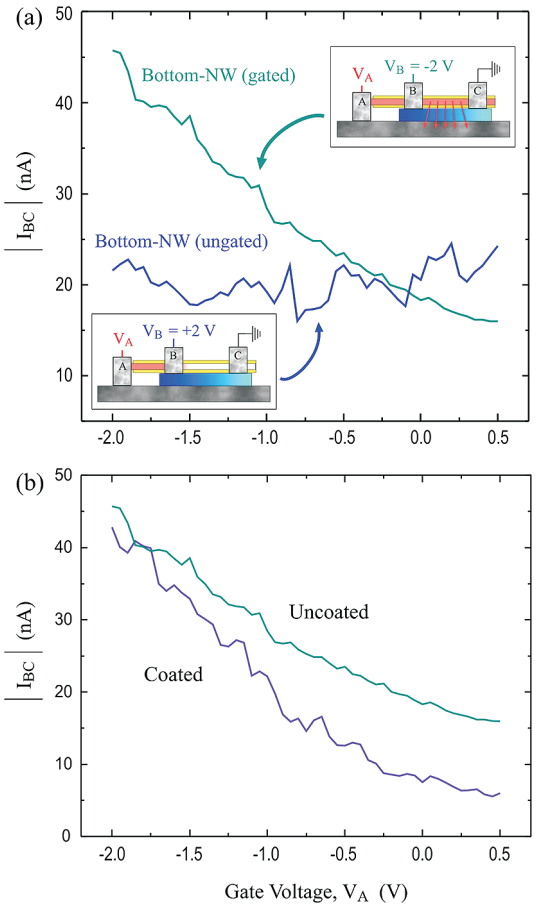

Figure 4. (a) Effect of gating the top-NW on the bottom-NW at $V_B = \pm 2$ V. For $V_B = -2$ V, a V_A sweep modulates the bottom-NW I_{BC}. For $V_B = +2$ V no modulation is observed, as the voltage does not propagate efficiently in the top-NW. (b) Al_2O_3 improves the top-NW gate efficiency.

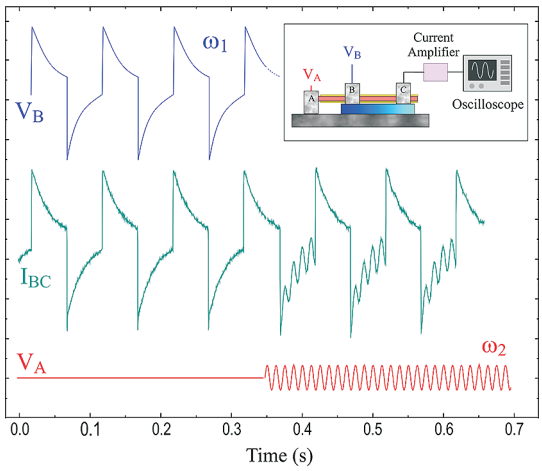

Figure 5. Analog signal processing with the CNWT. An arbitrary shaped curve of frequency $\omega_1 = 10$ Hz is supplied as V_B (blue curve). While the top-gate voltage $V_A = 0$, the bottom-NW current I_{BC} (green curve) follows V_B. When an ac voltage $\omega_2 = 80$ Hz is applied at V_A (red curve), the I_{BC} output is modulated, but only for negative V_B.

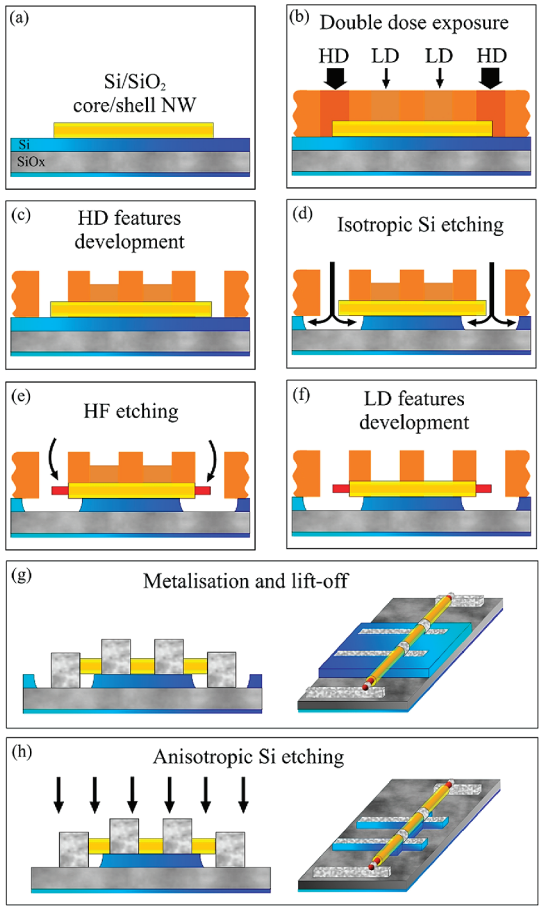

Figure 6. Step-by-step fabrication schematic of the CNWT.

with a p-type behavior (*i.e.*, the conductance decreases as the gate voltage increases). If the top-NW is off ($V_B = +2$ V), no modulation is seen. Hence, the CNWT behaves according to the circuit schematics in Figure 1d. With terminal C grounded ($V_C = 0$, Figure 4a), the transistor M3 is permanently on (Figure 3a) and the CNWT can be reduced to the basic circuit connections of the thyristor (Figure 1e). The graphs in Figure 4a present the behavior of a typical device. No significant variation is observed in between individual devices. To expand the operating range for V_A, a thicker oxide shell surrounding the top-NW must be used. Our ~10 nm thick oxide may show a non-negligible leakage current if a potential difference larger than ~3−4 V is applied between the two stacked NWs *via* any of the contacts.[31]

Figure 4b compares, for fixed $V_B = -2$ V, the I_{BC} modulation of a pristine CNWT (gated plot in Figure 4a) with the same device after deposition of a uniform 100 nm Al_2O_3 coating by atomic layer deposition, embedding the structure in a matrix with a dielectric constant ($\kappa \approx 9$)[36] higher than that of air. This passivates the surface and improves electrostatic coupling between the top- and bottom-NWs.[6,5] The bottom-NW conductance can then be varied to a greater extent with the top-NW gate (Figure 4b).

In Figure 5a single CNWT is exploited to generate analogue mixing between two ac waveforms. Using an

external generator, a waveform of frequency ω_1 is applied to terminal B (peak values ± 2 V), while a sine wave of frequency $\omega_2 > \omega_1$ is applied to terminal A (peak values ± 500 mV). The resulting envelope of I_{BC} is recorded by a digital oscilloscope *via* a current amplifier connected to terminal C (see circuit schematic in the inset of Figure 5). We use these waveform shapes to provide an effective visualization of the coupling. As long as $V_A = 0$ (left), I_{BC} follows the ac voltage drive V_B. When the sine wave is switched on at terminal A (right), an additional ω_2 modulation of I_{BC} appears, only when the ω_1 drive V_B is negative. The output waveform is thus the result of a complex signal processing well beyond the capabilities of a single transistor.

CONCLUSIONS

We exploited nanowire lithography to fabricate a novel building block where nanowire masks behave both as electrically active FETs and as interconnects, allowing the integration of two nanoscale transistors into a thyristor-like geometry. Such a device possesses an internal level of signal processing, particularly promising for analogue computation. The coupled nanowire transistor presented here is the simplest architecture achievable from a single nanowire mask *via* the nanowire lithography self-aligned process. An arbitrary sequence of electrodes can be devised to further expand the complexity, therefore the functionalities, of the basic device layout presented here.

METHODS

Device Fabrication. SiNWs are grown by Au-catalyzed vapor transport in a single-zone furnace tube.[30] Using a thin ($\sim$2–5 nm) Au catalyst layer, NWs with diameter $\sim$35–65 nm are obtained. These NWs comprise a $\sim$20–35 nm crystalline Si core, surrounded by a $\sim$10–15 nm SiO_2 shell.[31] SiNWs are transferred onto a SOI wafer (see Figure 6a) with the following structure: device layer: Si⟨100⟩, 50 nm, doping: p-type (B), resistivity: 20 Ωcm. Buried oxide: SiO_2, 150 nm. Handle: Si, 500 μm, doping: p-type (B), resistivity: 20 Ωcm.

A 500 nm polymethyl methacrylate resist is then spun on the as-dispersed SiNWs. An e-beam lithography pattern is prepared using a double-dose procedure (Figure 6b). This consists in exposing the features corresponding to electrodes B and C to a dose (0.7 mC/cm^2, low dose, LD) lower than that used for A and D (1.15 mC/cm^2, high dose, HD), so that they can be developed in separate steps.[31] The HD features are developed first, *via* a 10 s dip in 3:1 isopropyl alcohol/methyl isobutyl ketone (IPA:MIBK), leaving the LD features partially undeveloped (Figure 6c).

An isotropic Si etch removes the SOI layer at sites A and D, with a controllable $\sim$400 nm undercut, to avoid electrical contact between the top-NW electrodes and the SOI layer (Figure 6d). During this step, the SiO_2 shell of the SiNW protects the crystalline Si core, and the buried oxide layer acts as a vertical etch stop. We use deep reactive ion etching (Adixen AMS100) with SF_6 (250 sccm) etchant, 400 W rf power, 50 W bias power, 0.1 mbar pressure, and 30 s etch time.

The exposed SiO_2 NW shell at sites A and D is removed by a $\sim$10–13 s etch in buffered oxide etch solution (BOE), Figure 6e. The LD features are then developed by immersing the samples in a 1:1 IPA/MIBK solution for 30 s (Figure 6f). An O_2 plasma (100 W, 30 s) cleans the sample of development leftovers. Prior to metal deposition, an additional 3 s BOE dip restores a fresh Si surface at sites A and D,[31] which could have been compromised after the second development step, and removes the native oxide from the SOI surface at sites B and C. The dip is sufficiently short to prevent significant etching of the top-NW SiO_2 shell at sites B and C, so that this oxide can still be used as efficient gate dielectric.[31] The sample is transferred in a thermal evaporator where a 100 nm Ni film is deposited. Figure 6g shows the device after lift-off.

An anisotropic Si etching is finally performed *via* DRIE by means of a modified Bosch process[37] (Figure 6h). The procedure alternates short etch (SF_6, O_2) and passivation (C_4F_8) steps to minimize undercut (or scalloping)[29] and achieve a smooth sidewall profile for nanoscale vertical features.[21] Both top-NW and metal electrodes act as masks, so that their lateral morphology is transferred into the SOI layer, while all the exposed SOI areas are removed (Figure 6h).[21] The following conditions are used: main rf power: 400 W; bias power: 50 W; gases cycled: SF_6 (250 sccm)/C_4F_8 (200 sccm)/O_2(100 sccm); etch time per cycle: 0.8/1.2/1 s; pressure: 3×10^{-2} mbar; total etch time: 60 s.

To improve contact resistance, all devices are annealed in a 1:10 H_2/N_2 mixture at 1 bar. The temperature is ramped at 40 °C/min up to 350 °C, followed by 15 min dwell before cooling. Some devices are passivated with 100 nm Al_2O_3 deposited by ALD in a Beneq TFS 200 reactor. Deposition conditions are as follows: temperature: 200 °C; deposition cycle: 250 ms trimethylaluminum/500 ms purge/250 ms H_2O/500 ms purge; number of cycles: 1000; total dep. time: 25 min.

Electrical transport is measured with a Cascade Microtech probe station coupled to an Agilent B1500 device analyzer. The ac analogue response of the CNWT is assessed using an Agilent 33120A and an HP ESG-D3000A waveform generator, a Stanford Research SR570 current amplifier, and an LC334AM oscilloscope.

NWL with Core/Shell NW Masks. In the main text we reported electrical transport through the top-NW between electrodes A and D, proving that the Si/SiO_2 core/shell structure is a selective mask for shallow Si etching (the SOI is just 50 nm). The SiO_2 shell effectively prevents the crystalline core from suffering morphological damage, during both isotropic and anisotropic etch processes. This strategy is applicable for etch depths of up to several hundreds nanometers,[21] as the core/shell masks can survive much longer etch processes than those used here. As the etch depth approaches $\sim$2 μm, prolonged sputtering of the oxide shell eventually exposes the NW core, which is then etched away. As a consequence, the NW masks are no longer available for any "active" electrical purpose.

Acknowledgment. We acknowledge funding from ERC grant NANOPOTS, the Cambridge Integrated Knowledge Centre in Advanced Manufacturing Technologies for Photonics and Electronics, and the Cambridge Nokia Research Centre. A.C.F. is a Royal Society Wolfson Research Merit Award holder.

REFERENCES AND NOTES

1. International Technology Roadmap for Semiconductors, 2009 Edition, available online at http://www.itrs.net/.
2. Frank, D. J.; Dennard, R. H.; Nowak, E.; Solomon, P. M.; Taur, Y.; Wong, H.-S. P. Device Scaling Limits of Si MOSFETs and Their Application Dependencies. *Proceedings of the IEEE* **2001**, *89*, 259–288.
3. Barrett, C. R. The Digital Evolution–2006 MRS Spring Meeting Plenary Address. *MRS Bull.* **2006**, *31*, 906–913.
4. Li, Y.; Qian, F.; Xiang, J.; Lieber, C. M. Nanowire Electronic and Optoelectronic Devices. *Mater. Today* **2006**, *9*, 18–27.

5. Zhang, L.; Tu, R.; Dai, H. Parallel Core-Shell Metal-Dielectric-Semiconductor Germanium Nanowires for High-Current Surround-Gate Field-Effect Transistors. *Nano Lett.* **2006**, *6*, 2785–2789.
6. Hayden, O.; Bjork, M. T.; Schmid, H.; Riel, H.; Drechsler, U.; Karg, S. F.; Lortscher, E.; Riess, W. Fully Depleted Nanowire Field-Effect Transistor in Inversion Mode. *Small* **2007**, *3*, 230–234.
7. Zhong, Z.; Wang, D.; Cui, Y.; Bockrath, M. W.; Lieber, C. M. Nanowire Crossbar Arrays as Address Decoders for Integrated Nanosystems. *Science* **2003**, *302*, 1377–1379.
8. Whang, D.; Jin, S.; Lieber, C. M. Large-Scale Hierarchical Organization of Nanowires for Functional Nanosystems. *Jpn. J. Appl. Phys.* **2004**, *43*, 4465–4470.
9. Beckman, R.; Johnston-Halperin, E.; Luo, Y.; Green, J. E.; Heath, J. R. Bridging Dimensions: Demultiplexing Ultrahigh-Density Nanowire Circuits. *Science* **2005**, *310*, 465–468.
10. Krupke, R.; Hennrich, F.; von Löhneysen, H.; Kappes, M. M. Separation of Metallic from Semiconducting Single-Walled Carbon Nanotubes. *Science* **2003**, *301*, 344–347.
11. Li, X.; Zhang, G.; Bai, X.; Sun, X.; Wang, X.; Wang, E.; Dai, H. Highly Conducting Graphene Sheets and Langmuir-Blodgett Films. *Nat. Nanotechnol.* **2008**, *3*, 538–542.
12. Beecher, P.; Servati, P.; Rozhin, A.; Colli, A.; Scardaci, V.; Pisana, S.; Hasan, T.; Flewitt, A. J.; Robertson, J.; Hsieh, G. W.; *et al.* Ink-jet Printing of Carbon Nanotube Thin Film Transistors. *J. Appl. Phys.* **2007**, *102*, 043710.
13. Huang, Y.; Duan, X.; Cui, Y.; Lauhon, L. J.; Kim, K.-H.; Lieber, C. M. Logic Gates and Computation from Assembled Nanowire Building Blocks. *Science* **2001**, *294*, 1313–1317.
14. Lu, W.; Lieber, C. M. Nanoelectronics from the Bottom Up. *Nat. Mater.* **2007**, *6*, 841–850.
15. Likharev, K. K. Hybrid CMOS/Nanoelectronic Circuits: Opportunities and Challenges. *J. Nanoelectron. Optoelectron.* **2008**, *3*, 203–230.
16. Björk, M. T.; Ohlsson, B. J.; Thelander, C.; Persson, A. I.; Deppert, K.; Wallenberg, L. R.; Samuelson, L. One-Dimensional Heterostructures in Semiconductor Nanowhiskers. *Appl. Phys. Lett.* **2002**, *81*, 4458–4460.
17. Yang, C.; Zhong, Z.; Lieber, C. M. Encoding Electronic Properties by Synthesis of Axial Modulation-Doped Silicon Nanowires. *Science* **2005**, *310*, 1304–1307.
18. Borghetti, J.; Snider, G. S.; Kuekes, P. J.; Yang, J. J.; Stewart, D. R.; Williams, R. S. Memristive Switches Enable Stateful Logic Operations via Material Implication. *Nature* **2010**, *464*, 873–876.
19. Yun, W. S.; Kim, J.; Park, K. H.; Ha, J. S.; Ko, Y. J.; Park, K.; Kim, S. K.; Doh, Y. J.; Lee, H. J.; Salvetat; *et al.* Fabrication of Metal Nanowire Using Carbon Nanotube as a Mask. *J. Vac. Sci. Technol. B* **2000**, *18*, 1329–1332.
20. Myung, S.; Heo, K.; Lee, M.; Choi, Y. H.; Hong, S. H.; Hong, S. 'Focused' Assembly of V_2O_5 Nanowire Masks for the Fabrication of Metallic Nanowire Sensors. *Nanotechnology* **2007**, *18*, 205304.
21. Colli, A.; Fasoli, A.; Pisana, S.; Fu, Y.; Beecher, P.; Milne, W. I.; Ferrari, A. C. Nanowire Lithography on Silicon. *Nano Lett.* **2008**, *8*, 1358–1362.
22. Fasoli, A.; Colli, A.; Lombardo, A.; Ferrari, A. C. Fabrication of Graphene Nanoribbons via Nanowire Lithography. *Phys. Status Solidi B* **2009**, *246*, 2514–2517.
23. Bai, J.; Duan, X.; Huang, Y. Rational Fabrication of Graphene Nanoribbons Using a Nanowire Etch Mask. *Nano Lett.* **2009**, *9*, 2083–2087.
24. Liao, L.; Lin, Y. C.; Bao, M.; Cheng, R.; Bai, J.; Liu, Y.; Qu, Y.; Wang, K. L.; Huang, Y.; Duan, X. High-Speed Graphene Transistors with a Self-Aligned Nanowire Gate. *Nature* **2010**, *467*, 305–308.
25. Liao, L.; Bai, J.; Cheng, R.; Lin, Y. C.; Jiang, S.; Huang, Y.; Duan, X. Top-Gated Graphene Nanoribbon Transistors with Ultrathin High-k Dielectrics. *Nano Lett.* **2010**, *10*, 1917–1921.
26. Liao, L.; Bai, J.; Lin, Y. C.; Qu, Y.; Huang, Y.; Duan, X. High-Performance Top-Gated Graphene-Nanoribbon Transistors Using Zirconium Oxide Nanowires as High-Dielectric-Constant Gate Dielectrics. *Adv. Mater.* **2010**, *22*, 1941–1945.
27. Sze, S. M.; Ng, K. K. *Physics of Semiconductor Devices*, 3rd ed.; Wiley: Hoboken, 2007.
28. Kim, G.; Kim, M. K.; Chang, B.-S.; Kim, W. A. Low-Voltage Low-Power CMOS Delay Element. *IEEE J. Solid-State Circ.* **1996**, *31*, 966–971.
29. Fu, Y. Q.; Colli, A.; Fasoli, A.; Luo, J. K.; Flewitt, A. J.; Ferrari, A. C.; Milne, W. I. Deep Reactive Ion Etching as a Tool for Nanostructure Fabrication. *J. Vac. Sci. Technol. B* **2009**, *27*, 1520–1526.
30. Colli, A.; Fasoli, A.; Beecher, P.; Servati, P.; Pisana, S.; Fu, Y.; Flewitt, A. J.; Milne, W. I.; Robertson, J.; Ducati, C.; *et al.* Thermal and Chemical Vapor Deposition of Si Nanowires: Shape Control, Dispersion, and Electrical Properties. *J. Appl. Phys.* **2007**, *102*, 034302.
31. Colli, A.; Tahraoui, A.; Fasoli, A.; Kivioja, J.; Ferrari, A. C. Top-Gated Silicon Nanowire Transistors in a Single Fabrication Step. *ACS Nano* **2009**, *3*, 1587–1593.
32. Hsu, H.-C.; Wu, C.-Y.; Cheng, H.-M.; Hsieh, W.-F. Band Gap Engineering and Stimulated Emission of ZnMgO Nanowires. *Appl. Phys. Lett.* **2006**, *89*, 013101.
33. Appenzeller, J.; Knoch, J.; Tutuc, E.; Reuter, M.; Guha, S. Dual-Gate Silicon Nanowire Transistors with Nickel Silicide Contacts. *International Electron Devices Meeting* **2006**, *302*, 1–4.
34. Liu, B.; Wang, Y.; Ho, T.; Lew, K.-K.; Eichfeld, S. M.; Redwing, J. M.; Mayer, T. S.; Mohney, S. E. Oxidation of Silicon Nanowires for Top-Gated Field Effect Transistors. *J. Vac. Sci. Technol. A* **2008**, *26*, 370–374.
35. Whang, D.; Jin, S.; Lieber, C. M. Nanolithography Using Hierarchically Assembled Nanowire Masks. *Nano Lett.* **2003**, *3*, 951–954.
36. Kasap, S.; Capper, P., Eds. *Springer Handbook of Electronic and Photonic Materials*; Springer: New York, 2006.
37. Lärmer, F.; Schilp, A. *Method of Anisotropically Etching Silicon*. Patents DE 4241045, US 5501893, and EP 625285, 1994.